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315ball FBGA Specification

64Gb LPDDR5 (x32)

YM5XCBQ3B2-T16

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Feature

[LPDDR5x]

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2H = 1.05V (1.01V to 1.12V)
- VDD2L = 0.9V (0.87V to 0.97V)
- VDDQ = 0.5V (0.47V to 0.57V) or 0.3V (0.27V to 0.37V) (DVFSQ enabled)
- Programmable ODT for CK, CA, DQ, DMI, RDQS, WCK and with VSSQ termination
- Non-Target ODT for DQ
- VOH compensated output driver
- Double data rate command and address entry
- Double data rate architecture for data Bus;
  - two data accesses per clock cycle
- Differential clock inputs for command and address interface (CK_t, CK_c)
  - Single-ended CK selectable during low speed operation
- Differential clock inputs for data interface (WCK_t, WCK_c)
  - Single-ended WCK selectable during low speed operation
- Differential read data strobe (RDQS_t, RDQS_c)
  - Single-ended RDQS selectable during low speed operation
- Programmable Multi-bank organization (4Bank Groups/4Banks, 16Banks)
- DMI pin support for write data masking and DBIdc functionality
- Programmable RL (Read Latency) and WL (Write Latency)
- Burst length: 16 & 32
- Auto refresh and self refresh supported
- All bank auto refresh and directed per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) and PARC (Partial Array Refresh Control) by Bank Mask and Segment Mask
- Selectable background and command-based ZQ Calibration
- Dynamic Frequency and Voltage Scaling for Core and I/O (DVFSC and DVFSQ, respectively)
- Enhanced Dynamic Frequency and Voltage Scaling for Core (E-DVFSC)
- Optional Link ECC function
- Optional Data-Copy and Write-X functions
- 8B mode can be supported for LPDDR5x at 6400Mbps and below

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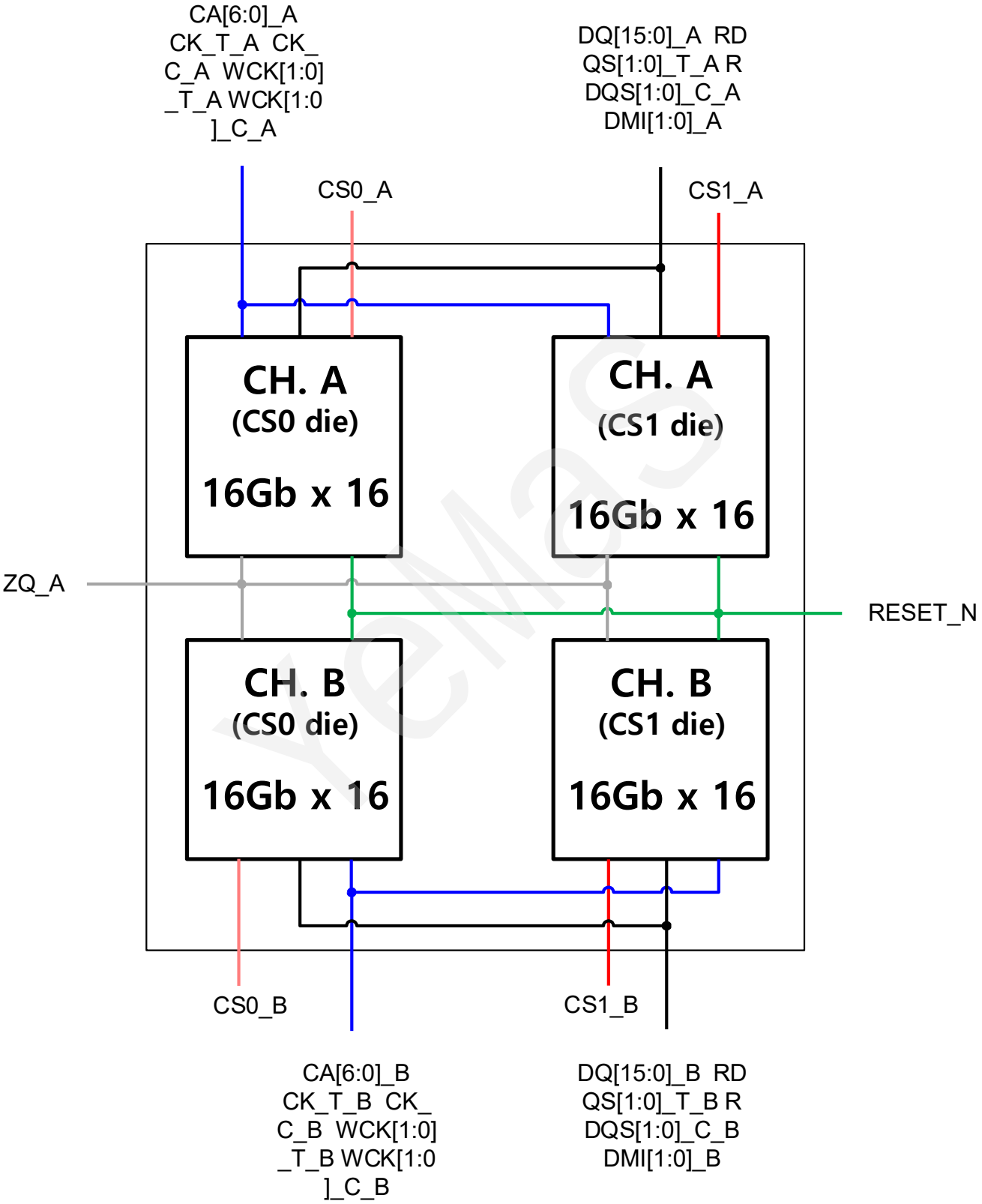
Functional Block Diagram



ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
YM5XCBQ3B2-T16	LPDDR5	1.8V/1.05/0.5	8GB (2CH 2CS)	6400	315Ball FBGA (Lead & Halogen Free)

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Package Information

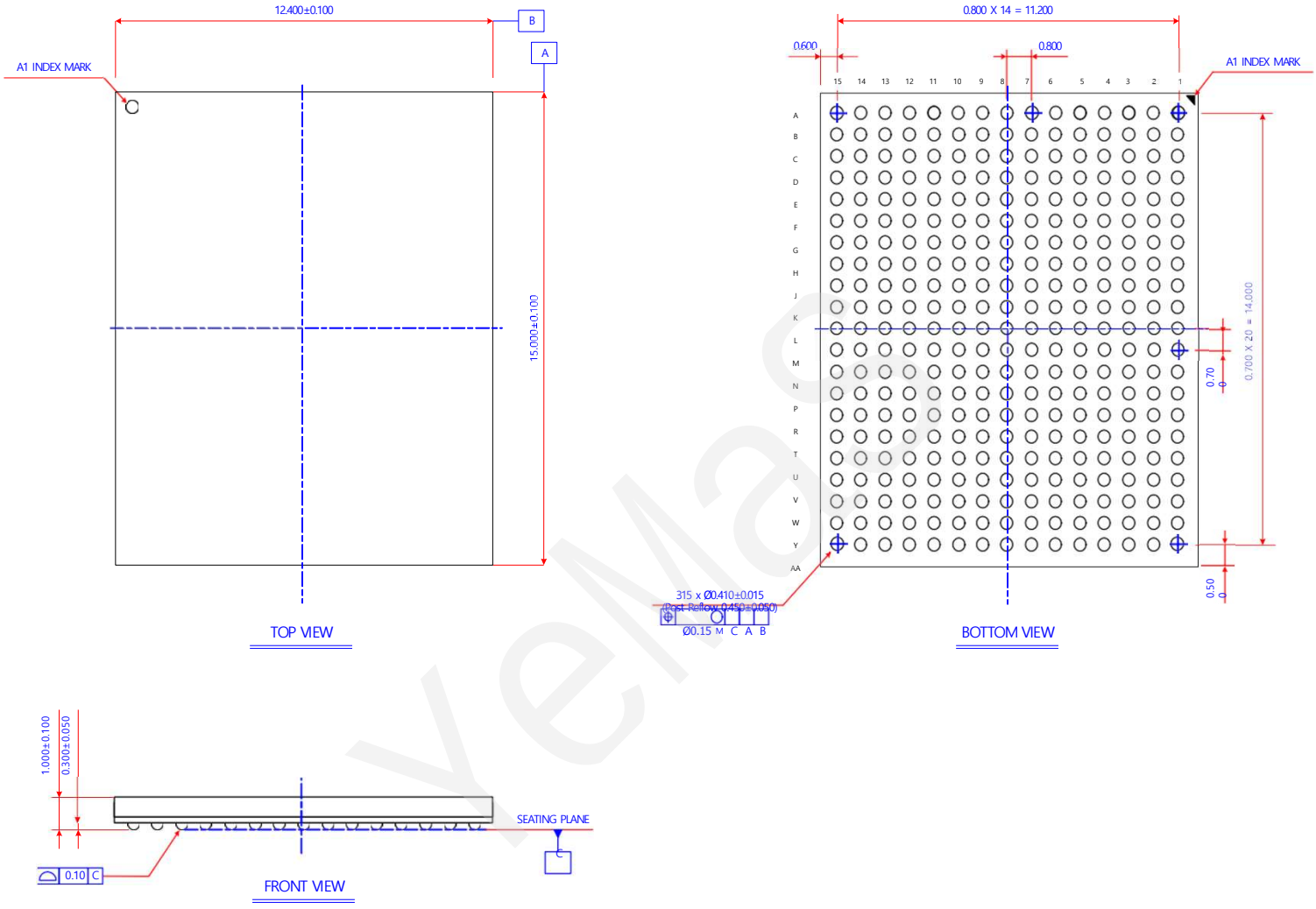
FBGA ballout - 315 balls, 12.4x15mm^2, 0.8/0.7mm pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	VDDQ	DMI0_A	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI1_A	VDDQ	NC	NC
B	NC	VDDQ	RDQS0_T_A	VSS	DQ4_A	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ12_A	VSS	RDQS1_T_A	VDDQ	NC
C	VDD1	DQ1_A	VDDQ	RDQS0_C_A	VSS	DQ5_A	VDD2H	VSS	VDD2H	DQ13_A	VSS	RDQS1_C_A	VDDQ	DQ9_A	VDD1
D	DQ0_A	VSS	DQ3_A	VDDQ	WCK0_C_A	VSS	VSS	VDD2H	VSS	VSS	WCK1_C_A	VDDQ	DQ11_A	VSS	DQ8_A
E	VSS	DQ2_A	VSS	WCK0_T_A	VDDQ	DQ6_A	VDD2H	VSS	VDD2H	DQ14_A	VDDQ	WCK1_T_A	VSS	DQ10_A	VSS
F	VDDQ	VSS	VDDQ	VDDQ	DQ7_A	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ15_A	VDDQ	VDDQ	VSS	VDDQ
G	VDDQ	VDDQ	VSS	CA0_A	VSS	CS1_A	VSS	CA2_A	VSS	CA4_A	VSS	CA6_A	VSS	VDDQ	VDDQ
H	Reset_N	VDD2L	VSS	VSS	CA1_A	VSS	CS0_A	VSS	CK_t_A	VSS	CA3_A	VSS	CA5_A	VDD2L	ZQ_A
J	VSS	VDD2L	VSS	RFU	VDD2H	RFU	VSS	VSS	CK_c_A	VSS	VDD2H	VSS	VSS	VDD2L	VSS
K	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
L	VSS	VSS	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VSS	VSS
M	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
N	VSS	VDD2L	VSS	VSS	VDD2H	VSS	CK_c_B	VSS	VSS	VSS	VDD2H	VSS	VSS	VDD2L	VSS
P	RFU	VDD2L	CA5_B	VSS	CA3_B	VSS	CK_t_B	VSS	CS0_B	VSS	CA1_B	VSS	VSS	VDD2L	RFU
R	VDDQ	VDDQ	VSS	CA6_B	VSS	CA4_B	VSS	CA2_B	VSS	CS1_B	VSS	CA0_B	VSS	VDDQ	VDDQ
T	VDDQ	VSS	VDDQ	VDDQ	DQ15_B	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ7_B	VDDQ	VDDQ	VSS	VDDQ
U	VSS	DQ10_B	VSS	WCK1_t_B	VDDQ	DQ14_B	VDD2H	VSS	VDD2H	DQ6_B	VDDQ	WCK0_T_B	VSS	DQ2_B	VSS
V	DQ8_B	VSS	DQ11_B	VDDQ	WCK1_c_B	VSS	VSS	VDD2H	VSS	VSS	WCK0_C_B	VDDQ	DQ3_B	VSS	DQ0_B
W	VDD1	DQ9_B	VDDQ	RDQS1_C_B	VSS	DQ13_B	VDD2H	VSS	VDD2H	DQ5_B	VSS	RDQS0_C_B	VDDQ	DQ1_B	VDD1
Y	NC	VDDQ	RDQS1_T_B	VSS	DQ12_B	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ4_B	VSS	RDQS0_T_B	VDDQ	NC
AA	NC	NC	VDDQ	DMI1_B	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI0_B	VDDQ	NC	NC

NOTE 1 0.8mm pitch (X-axis) 15 columns, 0.7mm pitch (Y-axis), 21 rows.
NOTE 2 Top View, A1 in top left corner.

Mechanical specification

315 Ball 0.8/0.7mm pitch 12.40mm x 15.00mm FBGA [t = 1.1mm max]



17. IDD Measurement

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

The values described below is the specification for 1ch based measurement.

Table - LPDDR5 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	6400 (x16)	Units	Notes
Operating one bank active-Precharge current: tCK = tCKmin; tRC = tRCmin; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD0_1$	VDD1	3.8	mA	9
	$IDD0_2$	VDD2H	22.4	mA	9
	$IDD0_2$	VDD2L	0.1	mA	9
	$IDD0_Q$	VDDQ	0.5	mA	3
Idle power-down standby current: tCK = tCKmin; Power-down entry command is issued CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2P_1$	VDD1	0.8	mA	
	$IDD2P_2$	VDD2H	3.4	mA	
	$IDD2P_2$	VDD2L	0.1	mA	
	$IDD2P_Q$	VDDQ	0.5	mA	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2PS_1$	VDD1	0.8	mA	
	$IDD2PS_2$	VDD2H	3.4	mA	
	$IDD2PS_2$	VDD2L	0.1	mA	
	$IDD2PS_Q$	VDDQ	0.5	mA	3
Idle non power-down standby current: tCK = tCKmin; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2N_1$	VDD1	0.8	mA	
	$IDD2N_2$	VDD2H	11.0	mA	
	$IDD2N_2$	VDD2L	0.1	mA	
	$IDD2N_Q$	VDDQ	0.5	mA	3

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Parameter/Condition	Symbol	Power Supply	6400 (x16)	Units	Notes
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2NS_1$	VDD1	0.8	mA	
	$IDD2NS_2$	VDD2H	10.9	mA	
	$IDD2NS_2$	VDD2L	0.1	mA	
	$IDD2NS_Q$	VDDQ	0.5	mA	3
Active power-down standby current: tCK = tCKmin; CS is LOW; One bank is active; Power-down entry command is issued CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD3P_1$	VDD1	1.3	mA	9
	$IDD3P_2$	VDD2H	8.0	mA	9
	$IDD3P_2$	VDD2L	0.1	mA	9
	$IDD3P_Q$	VDDQ	0.5	mA	3
Active power-down standby current with clock stop: Power-down entry command is issued CK_t=LOW, CK_c=HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD3PS_1$	VDD1	1.3	mA	9
	$IDD3PS_2$	VDD2H	8.0	mA	9
	$IDD3PS_2$	VDD2L	0.1	mA	9
	$IDD3PS_Q$	VDDQ	0.5	mA	4
Active non-power-down standby current: tCK = tCKmin; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD3N_1$	VDD1	1.4	mA	9
	$IDD3N_2$	VDD2H	16.3	mA	9
	$IDD3N_2$	VDD2L	0.1	mA	9
	$IDD3N_Q$	VDDQ	0.5	mA	4
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD3NS_1$	VDD1	1.4	mA	9
	$IDD3NS_2$	VDD2H	16.0	mA	9
	$IDD3NS_2$	VDD2L	0.1	mA	9
	$IDD3NS_Q$	VDDQ	0.5	mA	4

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Parameter/Condition	Symbol	Power Supply	6400 (x16)	Units	Notes
Operating burst WRITE current @ BG Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; One bank in each bank group 1 and 2 is active; BL = 16 or 32 ; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer RDQS_t is stable (if Link ECC is enabled) ODT disabled	$IDD4W_1$	VDD1	5.9	mA	
	$IDD4W_2$	VDD2H	257.5	mA	
	$IDD4W_2$	VDD2L	0.1	mA	
	$IDD4W_Q$	VDDQ	0.6	mA	4
Operating burst READ current @ BG Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; One bank in each bank group 1 and 2 is active; BL = 16 or 32 ; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	2.4	mA	
	$IDD4R_2$	VDD2H	294.8	mA	
	$IDD4R_2$	VDD2L	0.1	mA	
	$IDD4R_Q$	VDDQ	92.9	mA	8

All-bank REFRESH Burst current:
tCK = tCKmin;
CS is LOW between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching;
Data bus inputs are stable;
RDQS_t is stable (if Link ECC is enabled)
ODT disabled
WCK inputs are stable and static
	$IDD5_1$	VDD1	30.5	mA	

	$IDD5_2$	VDD2H	162.3	mA	
	$IDD5_2$	VDD2L	0.1	mA	
	$IDD5_Q$	VDDQ	0.5	mA	4

All-bank REFRESH Average current:
tCK = tCKmin;
CS is LOW between valid commands;
tRC = tREFI;
CA bus inputs are switching;
Data bus inputs are stable;
RDQS_t is stable (if Link ECC is enabled)
ODT disabled
WCK inputs are stable and static
	$IDD5AB_1$	VDD1	3.1	mA	

	$IDD5AB_2$	VDD2H	20.3	mA	
	$IDD5AB_2$	VDD2L	0.1	mA	
	$IDD5AB_Q$	VDDQ	0.5	mA	4

Per-bank REFRESH Average current:
tCK = tCKmin;
CS is LOW between valid commands;
tRC = tREFI/8;
CA bus inputs are switching;
Data bus inputs are stable;
RDQS_t is stable (if Link ECC is enabled)
ODT disabled
WCK inputs are stable and static
	$IDD5PB_1$	VDD1	3.1	mA	

	$IDD5PB_2$	VDD2H	20.5	mA	
	$IDD5PB_2$	VDD2L	0.1	mA	
	$IDD5PB_Q$	VDDQ	0.5	mA	4

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Parameter/Condition	Symbol	Power Supply	6400 (x16)	Units	Notes
Power down Self refresh current: CK_t=LOW, CK_c=HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable;	$IDD6_1$	VDD1	2.3	mA	6,7
	$IDD6_2$	VDD2H	12.8	mA	6,7
	$IDD6_2$	VDD2L	0.1	mA	6,7
Maximum 1x Self-Refresh Rate; (≤85° C) Maximum TBDx Self-Refresh Rate; (>85° C) RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD6_Q$	VDDQ	0.5	mA	4,6,7,8

Notes

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled. MR11 OP[6:4] = 000_B
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2H / VDD2L.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. The 1x Self-Refresh Rate is the rate at which the LPDDR5 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. When MR13 OP[7] is high, single VDD2 rail, VDD2L Current shall be added to VDD2H Current.
9. IDD values can be different according to the bank organization set by MR3 OP[4:3].
10. When DVFSC is enabled, the minimum tCK shall be set by following DVFSC operating frequency.

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